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10/678,710	10/03/2003	Chuan-Yi Lin	TSM03-0499	9881

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EXAMINER	
ROCCHEGIANI, RENZO	
ART UNIT	**PAPER NUMBER**
2825	

DATE MAILED: 09/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO 90C (Rev 10/03)

Office Action Summary	**Application No.** 10/678,710	**Applicant(s)** LIN ET AL.	
	Examiner Renzo N. Rocchegiani	**Art Unit** 2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 July 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 26-33 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,204,103 B1 (Bai et al.).

Bai et al. discloses a process to make a CMOS device comprising one step of siliciding a first source and drain region of a first transistor (item 1506, 1507 and col. 6, lines 40-44) on a substrate (item 1501) , and one step of siliciding a second source and drain region of a second transistor (item 1540, 1536 and col. 6, lines 40-47) on a substrate, forming a dielectric layer that is thinner than the gate electrodes of the transistrors (item 150) partially on the first and second source and drain regions, and siliciding the gate electrodes of the first and second transistors (Fig. 17-18), wherein the first gate electrode is fully silicided with TiSi2 (item 1602) and the second gate electrode is fully silicided with MoSi2 (Fig. 19). Furthermore, Bai et al. disclose partial silicidation of the gate electrodes during the silicidation of the respective source and drain regions (Fig. 15, items 1505 and 1532). The silicidation steps are performed by depositing a metal layer and then annealing. (col. 5, lines 38-50). A silicon oxide layer is formed over the previously formed dielectric layer. (item 1516). Also, the first transistor's source and drain regions are silicided with a metal different from the metal used to silicide the source and drain regions of the second transistor. (col. 5, lines 63-67 and col. 6, lines 1-5, wherein it is stated that the doped regions have work functions similar to those of their respective gates.)

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-12 and 34-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,204,103 B1 (Bai et al.) in view of U.S. Patent No. 6,074,915 (Chen et al.).

Bai et al. discloses a process to make a CMOS device comprising one step of siliciding a first source and drain region of a first transistor (item 1506, 1507 and col. 6, lines 40-44) on a substrate (item 1501), the first transistor comprising a gate electrode, with spacers formed alongside the gate electrode (items 1502 and 150), forming a dielectric layer (item 1516) on the first and second source and drain regions, the gate electrode and the spacers. The dielectric layer is then partially removed to uncover the top of the gate electrode, the gate electrode of the first transistor is then salicided (Fig. 17-18), wherein the first gate electrode is fully silicided with TiSi2 (item 1602). Furthermore, Bai et al. disclose partial silicidation of the gate electrode during the silicidation of the respective source and drain regions (Fig. 15, items 1505 and 1532). The silicidation steps are performed by depositing a metal layer and then annealing.

(col. 5, lines 38-50). Also, the first transistor's source and drain regions are silicided with a metal different from the metal used to silicide the source and drain regions of the second transistor. (col. 5, lines 63-67 and col. 6, lines 1-5, wherein it is stated that the doped regions have work functions similar to those of their respective gates.) Finally Bai et al. disclose forming an additional silicon dioxide dielectric layer over the dielectric layer formed over the transistor. (See Fig. 19, col. 7, lines 5-10).

Bai et al. does not teach that the first dielectric material formed over the source and drain regions, the gate electrode and the spacers is a nitrogen containing dielectric that may comprise a SiN or a SiON. Bai et al. also does not teach that the metal layers used to form the silicides may comprise a plurality of layers.

Chen et al. teach the formation of dielectric layer over source and drain regions, the gate electrode and the spacers using silicon nitride or silicon oxynitride in place of silicon oxide. (col. 9, lines 55-60).

It would have been obvious to form the dielectric of a nitrogen containing layer such as silicon nitride or silicon oxynitride, since Chen et al. teaches that these are well known materials used in the art to form interlevel dielectric and that these materials are interchangeable with silicon oxide which is what Bai et al. discloses as using. Furthermore, it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

While Bai et al. only discloses a single layer of metal for the formation of the silicide it would have been obvious to one with ordinary skill in the art to deposit a plurality of layers as opposed to a single thick layer of metal to form the silicide, since it has been held that constructing a formerly integral structure in various elements involves only routine skill in the art. *Nerwin v. Erlichman*, 168 USPQ 177, 179.

5. Claims 13-23 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,204,103 B1 (Bai et al.).

As stated in paragraph 2, all the limitations of these claims have been met except for teaching that the silicidation steps to fully silicide the gate electrodes are performed separately and that the metal layers used during this silicidation processes may comprise multiple metal layers.

Even though Bai et al. discloses the silicidation step of the two gates to be simultaneous, it would have been obvious to one with ordinary skill in the specific art to split this step into two separate steps, since in general, the transposition of process steps or the splitting of one step into two, where the processes are substantially identical or equivalent in terms of function, manner and result, has been held to not patentably distinguish the process. *Ex parte Rubin*, 128 USPQ 159.

Also, while Bai et al. only discloses a single layer of metal for the formation of the silicide it would have been obvious to one with ordinary skill in the art to deposit a plurality of layers as opposed to a single thick layer of metal to form the silicide, since it has been held that constructing a formerly integral structure in various elements involves only routine skill in the art. *Nerwin v. Erlichman*, 168 USPQ 177, 179.

6. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,204,103 B1 (Bai et al.) in view of U.S. Patent No. 6,150,243 (Wieczorek et al.).

As stated in paragraph 5, all the limitiations of these claims have been met except for teaching that the dielectric layer may comprise a silicon nitride or a silicon oxynitride.

Wieczorek et al. teach the formation of sidewall spacers over source and drain regions using silicon nitride or silicon oxynitride. (col. 6, lines 5-15).

It would have been obvious to form the sidewall spacers of silicon nitride or silicon oxynitride, since Wieczorek et al. teaches that these are well known materials used in the art to form sidewall spacers and since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

Response to Arguments

7. Applicant's arguments with respect to claims 1-41 have been considered but are moot in view of the new ground(s) of rejection. In the last response applicant amended each of the independent claims by adding a different limitation to each claim in an attempt to overcome the prior art. While the amendment resulted in overcoming the rejection as presented in the previous office action, upon reconsideration of the prior art and the addition of the new reference US Patent No. 6,074,915, the examiner has realized the even with the amendments the claims are either anticipated or rendered

obvious by the prior art. Because all the claims can be easily referred to by addressing each of the three amendments, the following arguments will be organized in three sections each one addressing a different amendment made to the claims. Furthermore, since applicant's arguments mainly address the independent claims, the following remarks will do the same, with the understanding that the dependent claims fall in the same groups as the independent claims upon which they depend.

With respect to the amendment that ads the language of "forming a nitrogen containing .... The source region and the drain region" that was added to claim 1 and that is found in newly added independent claim 34, this language overcomes the 102 rejection over Bai but still does not render the claims patentable. This language narrows the scope of the claims in that it specifies that the dielectric layer that is a nitrogen containing layer is not the sidewall spacers, and instead it is the interlevel dielectric. The reference to Bai only discloses forming a silicon oxide as the interlevel dielectric layer thus the reference to Bai no longer anticipates claim 1. Yet, combined with the newly added reference US Patent No. 6,074,915, Bai renders this limitation obvious. The '915 patent teaches that interlevel dielectric layers may be formed of silicon oxide or nitrogen containing layers such as silicon nitrides or silicon oxynitrides. Because of this teaching one with ordinary skill in the specific art would be motivated to substitute the material and still have an expectation of success. Thus, while the amendment has overcome the 102 rejection, it still does not render the claims patentable because the limitation added is an obvious one.

With respect to the limitation added to claim 13, i.e. the language that recites "siliciding the second gate electrode ... of siliciding the first gate electrode" this limitation also results in overcoming the 102 rejection with respect to claim 13, but still does not render the claim patentable. This limitation as the previously discussed one is also rendered obvious by the prior art. There is established case law that has held that splitting one step into two is obvious when the function, manner and result are the same. The present instance is such a case. The prior art, namely Bai teaches the silicidation to be a simultaneous annealing step. The splitting of this step into two would not change the function, manner and result of the process. If one were to deposit the Ti layer over one gate and then anneal, and then deposit the Mo layer over the second gate and then anneal, the result would be the same. This is because the function of these metal layers that salicide the gate electrodes is the same whether the process if performed simultaneously or in two separate steps. Thus, this limitation again is rendered obvious by the prior art and thus does not render the claim allowable.

Thirdly, with respect to the limitation added to claim 26, i.e. the language that recites "a dielectric layer having a thickness . . . the first and second transistors" this limitation does not overcome the previously presented rejection. As the rejection in the previous action took into consideration that the claims as broadly worded could reasonably be interpreted to refer to the sidewall spacers when reciting the limitation of "dielectric layer", the same interpretation would allow for Bai to anticipate the amended claim 26. Considering the sidewall spacers in the Bai reference to be the dielectric layer recited in claim 26, the spacers do have a thickness that is less than the gate electrode.

Thus, the prior art still anticipates claim 26 including the newly added limitation. The examiner would like to further point out that the same interpretation with respect to the dielectric layer being the sidewall spacers in the Bai reference used to anticipate claim 26, is still been applied to also claim 13. Thus, the 103 rejection of claim 24 is also the same rejection as was presented in the previous office action. This is different from the interpretation given to Bai used in the rejection of claim 1 and 34 as explained above.

For the above reasons, the claims of the pending application stand rejected.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Renzo N. Rocchegiani whose telephone number is (571)272-1904. The examiner can normally be reached on Mon.-Fri. 8:00 am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571)272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Renzo N. Rocchegiani
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Art Unit 2825

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